

REMARKS

Claims 1, 4 and 7 are amended. New claims are added. No new subject matter is added. Claims 1-8 remain pending the application. Reconsideration and allowance of the pending claims is requested in light of the following remarks.

Claim Amendments

The amendments to claim 1 are fully supported by the original application at, e.g., FIGs. 2A, 2B, 4B, and page 7, lines 6-8.

The amendments to claim 4 are fully supported by the original application at, e.g., FIG. 2B.

The amendments to claim 7 are fully supported by the original application at, e.g., FIGs. 2A, 2B, 4B, and page 7, lines 6-8.

Claim Rejections – 35 U.S.C. § 103

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,424,011 to Assaderaghi, et al. ("Assaderaghi") in view of U.S. Patent No. 5,767,549 to Chen, et al. ("Chen"). The applicant disagrees.

Claim 1 recites a semiconductor layer, and it has been alleged that Assaderaghi's SOI layers of FIGs. 5a-5l (clearly labeled "SOI") correspond to the recited semiconductor layer. Claim 1 further recites that the SOI layer includes an active area and a device isolation area, the device isolation area consisting of a well, where the well includes additional impurity ions compared to the active region.

Assaderaghi's multiple SOI layers are separated by shallow isolation regions 202 (FIG. 5a; column 9, lines 61-67). Assaderaghi FIGs. 2a and 5e illustrate that the SOI layers are coextensive with the source/drain regions 20, 22. In other words, the SOI layers are located entirely in the active region that is defined by the source/drain regions 20, 22 (FIG. 2a). No part of Assaderaghi's SOI layer is disposed in the device isolation areas, which is the region having the STIs 26, 28. Since it is well-known that shallow trench isolation regions are composed of insulative material rather than semiconductor material, it is incorrect to interpret Assaderaghi's shallow trench isolation regions 26, 28 as being included in, or part of, the SOI layer.

It is alleged in the advisory action that the continuous nature of the applicant's SOI region is irrelevant since such a feature is not specifically claimed. The applicant would

point out that claim 1 *explicitly recites* that the SOI layer includes an active area and a device isolation area, and that the meaning of words used in a claim is not construed in a lexicographic vacuum, but *in the context of the specification and the drawings*. MPEP 2111.02(III). The continuous nature of the applicant's SOI region was identified so that the explicitly recited features of the claim could be construed in their proper context.

Thus, Assaderaghi fails to teach that any one of the multiple SOI layers includes a device isolation area.

It was further alleged in the advisory action that "it is not particularly relevant whether the STI structures of Assaderaghi are considered to be inside the SOI layer, since Assaderaghi, when combined with Chen, provides a structure in which a portion of the SOI layer remains underneath the isolation structure." Thus, the Examiner recognizes that Chen's "isolation structure" (field oxide 38, FIG. 1) is separate from Chen's "SOI layer" (single crystal semiconductor material 18, FIG. 1).

However, also contrary to claim 1, Chen does not teach that the portion of Chen's SOI layer that remains underneath the isolation structure consists of a well.

Claim 1 further recites an insulating layer disposed on an upper surface of the field oxide film.

Contrary to this feature of claim 1, it was recognized that Assaderaghi fails to teach a field oxide film as recited in claim 1. Chen also fails to show an insulating layer disposed on an upper surface of a field oxide film.

Claim 1 further recites that the well includes additional impurity ions compared to the active area. It was recognized that Assaderaghi does not disclose a well. Furthermore, Chen does not teach that the portion of the single crystal semiconductor material layer 18 (FIG. 1) that remains underneath the isolation structure has additional impurity ions compared to the active region of the single crystal semiconductor material layer 18.

For any one of the above reasons, the combination of Assaderaghi and Chen does not establish *prima facie* obviousness for claim 1 because it fails to teach or suggest all the features recited in the claim. MPEP 2143.03.

Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Assaderaghi in view of Chen and U.S. Patent No. 5,026,666 to Hills, et al. ("Hills"). The applicant disagrees.

Claim 4 recites a metal fill disposed in contact with the insulation layer, in contact with an upper surface and the sidewall of the gate line, and in contact with an upper surface of the first active area. Neither Assaderaghi, Chen, nor Hills teach that the metal fill is disposed in contact with an upper surface and the sidewall of the gate line.

For this reason the combination of Assaderaghi, Chen and Hills fails to establish *prima facie* obviousness for claim 4 because it does not teach all the features recited in the claim. MPEP 2143.03.

Claim 4 additionally recites an insulation layer disposed on the first active area and disposed on the field oxide layer, the insulation layer in contact with a sidewall of the gate line.

The applicant refutes the two specific assertions made in the final office action on page 5, first paragraph, that "gate spacer layers (conformal layers 210) can reasonably be considered to be part of the gate line or alternatively part of the insulation layer [211] (since both are typically silicon oxide)."

Gate spacer layers cannot be reasonably considered part of the gate line, since, as has been recognized, gate spacer layers are typically insulative in nature, rather than conductive in nature as gate lines are well-known to be.

As for the second, alternate assertion, it amounts to a statement that a gate spacer is inherently part of a surrounding insulation layer because gate spacers and insulation layers are typically both made of the same material.

The applicant agrees that gate spacers and the surrounding insulation layer may be made of the same material, but this is not necessarily always the case. For example, it is known that gate spacers are often made of a different material than a surrounding insulation layer in order to achieve different etch rates and protect the gate when an etch is occurring in the surrounding insulation layer. The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. MPEP 2112(IV), emphasis in original. Thus, gate spacers cannot inherently be considered part of a surrounding insulation layer.

Regarding the Hills reference, it is suggested that Hills provides the teaching to omit the gate spacers of Assaderaghi because Hills regards the gate sidewall oxide spacers 129-130 as purely optional in order to provide for LDD structures (column 2, lines 25-30).

As was identified by the Examiner, Assaderaghi does teach LDD structures (column 12, line 67), and further submits that Assaderaghi shows dopant regions that have a shape characteristic of regions including LDD portions. Assaderaghi additionally teaches that in order to implement NVRAM (flash), DRAM, or SRAM circuits, three additional process steps are *required* (column 12, lines 63-64; emphasis added). These three steps include thicker gate oxide, special LDD, and deeper junction implant (column 12, lines 66-67). Thus, Assaderaghi teaches that LDD is not optional.

Therefore, if one adopts the position that the only purpose for gate spacers is to form LDD structures, Hills does not provide motivation to remove the gate spacers from Assaderaghi. This is because Assaderaghi indicates, as explained above, that the LDD process is required for the NVRAM, DRAM, and SRAM structures. Thus, Assaderaghi requires the use of gate spacers to form the LDD structures. Eliminating Assaderaghi's gate structures according to Hills would make it impossible to form the required LDD structures, and would therefore render Assaderaghi unsuitable for its intended purpose. In such a situation there can be no suggestion or motivation to combine the references. MPEP 2143.01.

Since there is no motivation or suggestion to modify Assaderaghi with Hills in the manner that is suggested, a *prima facie* case of obviousness is not established by the combination of Assaderaghi, Chen and Hills. MPEP 2143.

Claims 5-6 are allowable over the combination of Assaderaghi, Chen and Hills at least because any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03.

Regarding claim 7, it recites features that are similar to claims 1 and 4. Consequently, the comments made above for claims 1 and 4 apply with equal weight to claim 7.

Additionally, claim 7 recites that the field oxide layer is in contact with the well and is horizontally coextensive with the well. Neither Assaderaghi, Chen, nor Hills show, teach or suggest a field oxide layer that is in contact with a well or that is horizontally coextensive with the well.

Claim 8 is allowable over the combination of Assaderaghi, Chen and Hills at least because any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03.

Conclusion

For the above reasons, reconsideration and allowance of the pending claims is requested. Please telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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